1st Sem Digital Electronics

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12EC121

First Semester M.Tech. Degree Examination, February 2013
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain abstraction with example. **(04 Marks)**

b. Describe the design methodology for hardware/software codesign with flowchart. **(08 Marks)**

c. Develop a sequential circuit that has a single data input signal, 'S' and produces an output 'Y'. The output is '1' whenever 'S' has the same value over three successive clock cycles, and '0' otherwise. Assume that the value of 'S' for a given clock cycle is defined at the time of the rising clock edge at the end of the clock cycle. **(08 Marks)**

2 a. Explain the concept of parity error checking. Discuss the parity trees for generating and checking even parity to augment an 8-bit code. **(08 Marks)**

b. Discuss BCD code and 7-segment decoders. **(04 Marks)**

c. Develop a verilog model for a 7 segment decoder. Include an additional input bank, that overrides the BCD input and causes all segments not to be lit. **(08 Marks)**

3 a. Explain the operation of resizing unsigned integers. **(08 Marks)**

b. Develop a verilog model of a code converter to convert the 4 bit gray code to a 4-bit unsigned binary integer. **(07 Marks)**

c. Write verilog module declaration for a code converter that has an input representing an unsigned number in the range 0 to 48 with a precision of at least 0.01, and an output representing a signed number in the range – 100 to 100 with a precision of at least 0.01. **(05 Marks)**

4 a. Describe the operation of latch with timing diagram and verilog model. **(06 Marks)**

b. Design a circuit for a modulo 10 counter known as decade counter. Also develop a verilog model for the same. **(08 Marks)**

c. Describe Finite State Machines (FSM) with schematic representation. **(06 Marks)**

5 a. Explain flow through SSRAM and pipelined SSRAM with verilog models. **(08 Marks)**

b. Determine whether there is an error in the ECC word 000111000100, and if so, correct it. **(06 Marks)**

c. What is field programmable gate arrays (FPGAs)? With a diagram explain the internal organization of an FPGA. **(06 Marks)**

6 a. Explain with block diagram, the organization of high performance embedded computer with multiple busses. **(07 Marks)**

b. What is meant by the term little-endian and big-endian memory layout for data words? **(04 Marks)**

c. Suppose the value in data memory location 100 represents the number of seconds elapsed in a time interval. Write instruction to increment the value, wrapping around to 0 when the value increments above 59. **(03 Marks)**

d. Explain cache memory in processor. What are the advanced techniques used to enable a higher rate of transfer or memory bandwidth. **(06 Marks)**

7 a. With a neat diagram, explain the R/2R ladder DAC. **(05 Marks)**

b. Discuss the three basic ways to synchronize transmitter and receiver in a serial transmission. **(09 Marks)**

c. Discuss two schemes for implementing parallelism in acceleration. **(06 Marks)**

8 a. Describe the three properties of design such as area, timing and power for design optimization. **(12 Marks)**

b. Describe the built-in-self-test (BIST) technique used in design for test. **(08 Marks)**

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